Solution

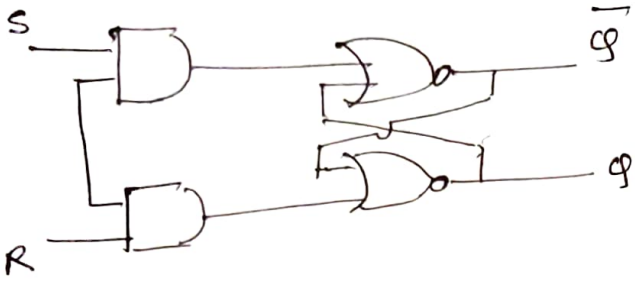
Branch : Electronics

Date 18/07/2022

First half 2022 (Supplementary)

Q(4)(b) Design SR Latch using any MOS design style.

Clocked & NOR based SR latch



$\overline{Q} = \overline{S\,clk + Q}$

$Q = \overline{R\,clk + \overline{Q}}$

(Draw complex ckt)

Q(4)(a) Explain 4 bit CLA adder with its carry eqn. Draw MODL

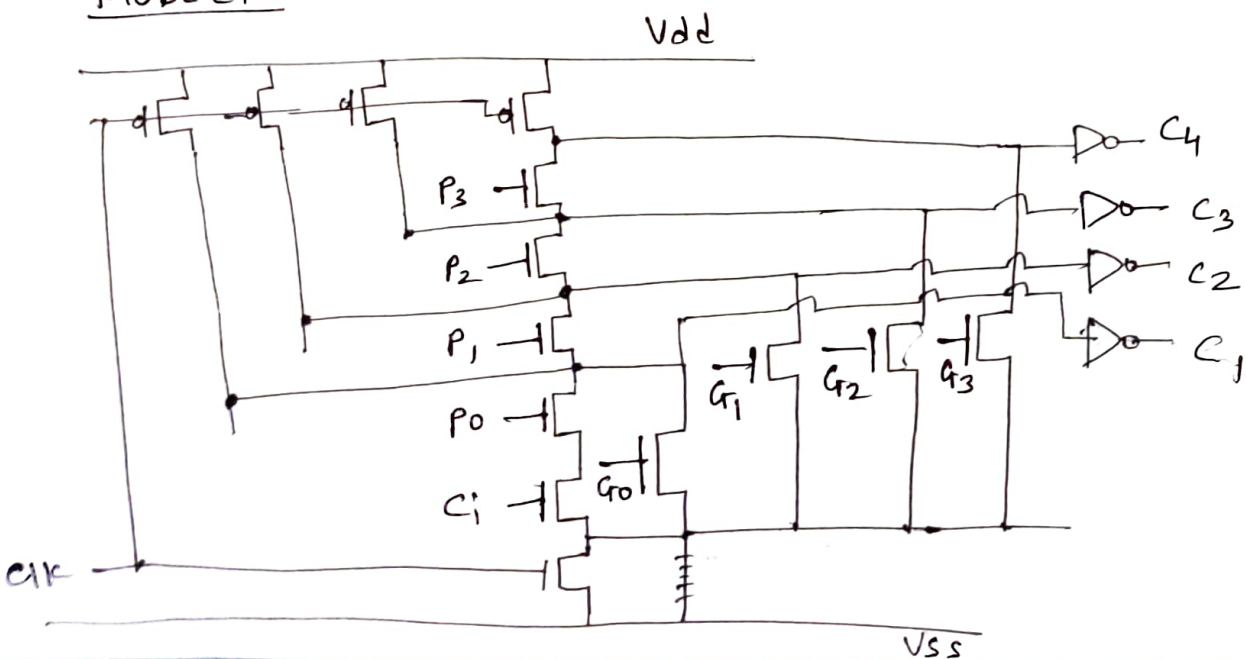
4 bit CLA ckt.

$\overline{C_1} = \overline{G_0 + P_0 C_i}$ $\quad \overline{C_2} = \overline{G_1 + P_1 G_0 + P_1 P_0 C_i}$

$\overline{C_3} = \overline{G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_i}$

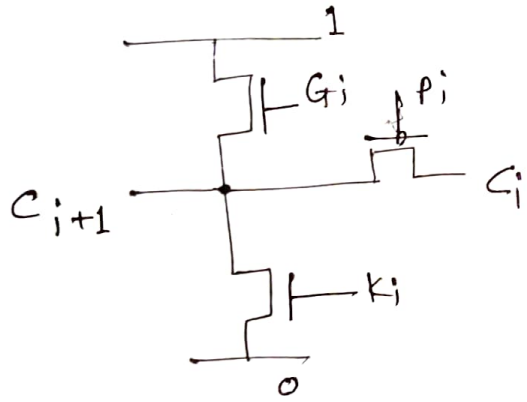
$\overline{C_4} = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_i}$

MODL CKT



Q ① (d) Explain basic Manchester carry ckt with suitable diagram.

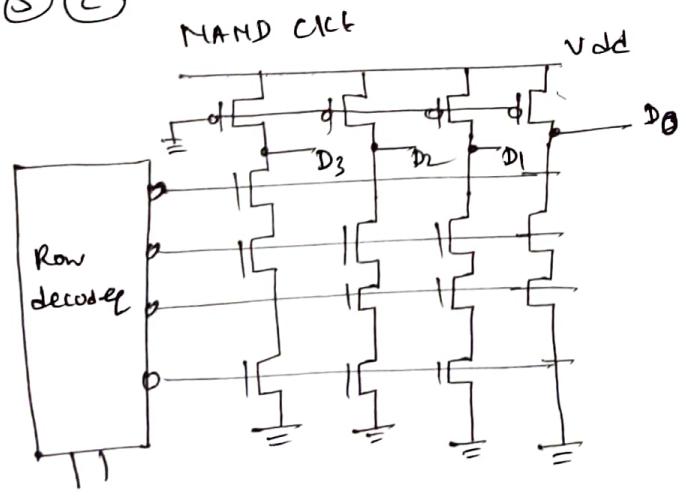
A_i	B_i	$P_i = A_i \oplus B_i$	$G_i = A_i B_i$	$K_i = \overline{A_i + B_i}$
0	0	0	0	1
0	1	1	0	0
1	0	1	0	0
1	1	0	1	0

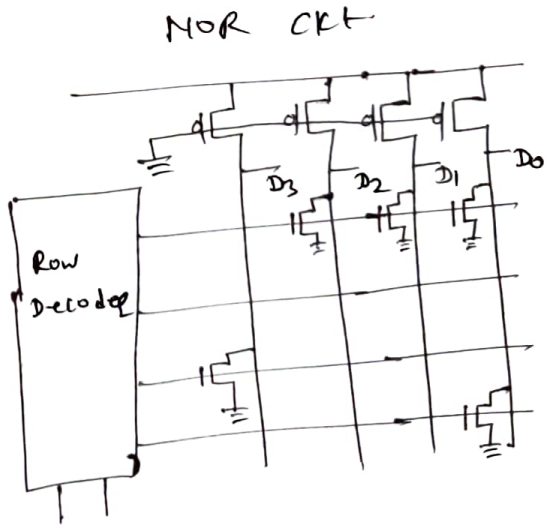


Switch n/w for the carry-out equation.

(Draw ckt for 4 bits)

Q ⑤ (c)





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Draw MOSFET for 1